ABSTRACT OF THE DISCLOSURE

A method and apparatus to create bypass logic in a digital circuit design comprising coupling a first latency delay unit to a data input of the conditional state element (e.g., a flip-flop). Coupling a second latency delay unit to an enable input of the conditional state element. Coupling a first input of a multiplexer to an output of the conditional state element. Coupling a second input of the multiplexer to the data input of the conditional state element; and coupling a select line of the multiplexer to the enable input of the conditional state element to form a logically redundant element. Replacing the conditional state element in a feedback loop of a finite state machine with the logically redundant element and manipulating latency delay units to create bypass logic in the digital circuit design.